PEEL™ 22V10AZ (5V), 22V10AZ3 (3V) Zero Power CMOS Programmable Electrically Erasable Logic Device

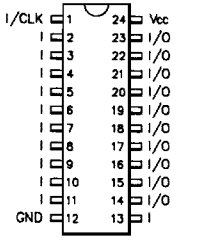
Features

- **Low Power, Low Voltage**
  - — I_{CC} = 10μA standby
  - — V_{CC} = 4.75V - 5.25V for 22V10AZ
    V_{CC} = 2.70V - 3.60V for 22V10AZ3
  - — t_{PD} = 15ns and 25ns versions
- **Electrically Erasable Technology**
  - — Superior factory testing
  - — Reprogrammable in plastic package
  - — Reduces retrofit and development costs
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT PLACE Development Software and PDS-3 programmer
- **Architectural Flexibility**
  - — 132 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
  - — 24-pin DIP, SOIC and 28-pin PLCC packages
- **Application Versatility**
  - — Replaces random logic
  - — Pin compatible with standard 22V10
  - — Ideal for power-sensitive systems
  - — Enhanced architecture options

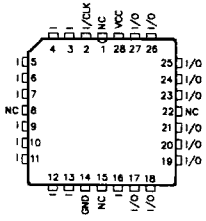
General Description

The PEEL22V10AZ and PEEL22V10AZ3 are Programmable Electrically Erasable Logic (PEEL) devices providing low power and low voltage alternatives to ordinary PLDs. The PEEL22V10AZ and PEEL22V10AZ3 are available in 24-pin DIP, SOIC, and 28-pin PLCC packages. A "zero-power" standby mode, makes the PEEL22V10AZ and PEEL22V10AZ3 ideal for power sensitive applications such as hand held meters, portable communication equipment and laptop computer/peripherals. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL22V10AZ and PEEL22V10AZ3 are JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e, 22V10AZ+). The additional macro cell configurations allow more logic to be put into every design. Development and programming support for the PEEL22V10AZ and PEEL22V10AZ3 is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

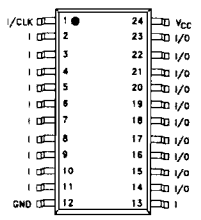
Pin Configuration (Figure 1)



DIP

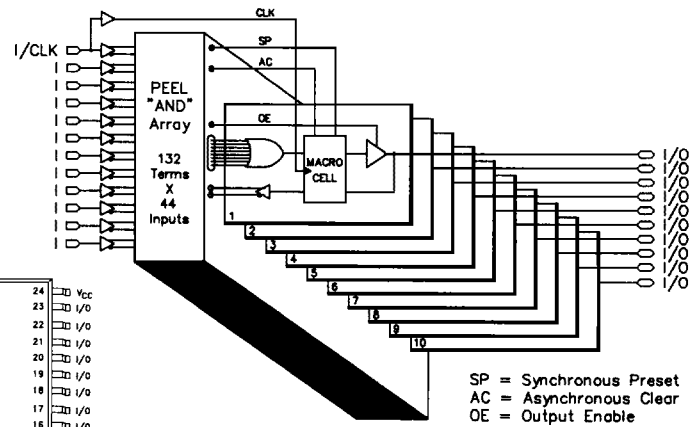


PLCC



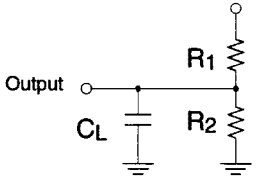
SOIC

Block Diagram (Figure 2)

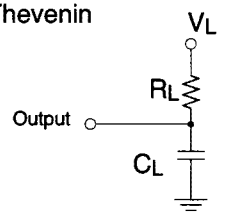


PEEL Device and PEEL Array Test Loads

Standard Load



Thevenin



Part Number	Standard Loads				
	CMOS Interface		TTL Interface		
	R1	R2	R1	R2	C_L
PEEL18CV8	480KΩ	480KΩ	235Ω	159Ω	50pF
PEEL20CG10A	480KΩ	480KΩ	235Ω	159Ω	50pF
PEEL22CV10A	480KΩ	480KΩ	235Ω	159Ω	50pF
PA7024	480KΩ	480KΩ	235Ω	159Ω	50pF
PA7128	480KΩ	480KΩ	235Ω	159Ω	50pF
PA7140	480KΩ	480KΩ	235Ω	159Ω	50pF

Part Number	Thevenin Equivalent				
	CMOS Interface		TTL Interface		
	R_L	V_L	R_L	V_L	C_L
PEEL18CV8	228KΩ	2.375V	95Ω	2.02V	50pF
PEEL20CG10A	228KΩ	2.375V	95Ω	2.02V	50pF
PEEL22CV10A	228KΩ	2.375V	95Ω	2.02V	50pF
PA7024	228KΩ	2.375V	95Ω	2.02V	50pF
PA7128	228KΩ	2.375V	95Ω	2.02V	50pF
PA7140	228KΩ	2.375V	95Ω	2.02V	50pF